## WHAT IS CLAIMED IS:

1. A circuit for combining on/off key and warm boot key to obtain a function of cold boot key in a portable information device, comprising:

a first switch circuit, which is controlled by the on/off key for turning on and off;

a second switch circuit, which is connected to the first switch circuit and controlled by the warm boot key for turning on and off; and

a switch driving circuit, which is connected in parallel with the first switch circuit and the second switch circuit and has an output terminal connected to a reset pin of a central processing unit (CPU), such that the switch driving circuit is turned on when the first switch circuit and the second switch circuit are simultaneously turned off, and the output terminal thus outputs a signal to cold boot the portable information device.

2. The circuit as claimed in claim 1, wherein the on/off key connected by the first switch circuit provides a sleeping mode to display latest system information before shut-down on a screen of the portable information device as soon as system re-starts.

3. The circuit as claimed in claim 1, wherein the warm boot key connected by the second switch circuit sends an interrupt signal to the CPU when system re-boots, so as to store system information in memory and clear temporary data in the memory.

4. The circuit as claimed in claim 1, wherein each of the first switch circuit, the second switch circuit and the switch driving circuit consists of an NMOSFET.

5. The circuit as claimed in claim 4, wherein drains of the first switch circuit and the second switch circuit are connected in parallel and connected to a gate of the switch driving circuit.

6. The circuit as claimed in claim 4, wherein sources of the first switch circuit, the second switch circuit and the switch driving circuit are all grounded directly.

7. The circuit as claimed in claim 1, wherein the first switch circuit has a line connected to a first pin of interrupt signal of the CPU, to send an interrupt signal to the CPU for reset.

8. The circuit as claimed in claim 1, wherein the second switch circuit has a line connected to a second pin of interrupt signal of the CPU, to send an interrupt signal to the CPU.